International
IOR Rectifier

IRS2092

PROTECTED DIGITAL AUDIO AMPLIFIER

Features

- Integrated analog input Class D audio amplifier driver in a small 16 pin package
- Floating inputs enable easy half bridge implementation
- Programmable bidirectional over-current protection with self-reset function
- Programmable preset deadtime for improved THD performances
- Start and stop click noise reduction
- High noise immunity
- ±100 V ratings deliver up to 500 W in output power
- Operates up to 800 kHz
- RoHS compliant

Product Summary

V_{OFFSET} (max)		± 100 V
Gate driver	Io+	1.0 A
	Io -	1.2 A
Selectable Deadtime		25/40/65/105 ns
OC protection delay (max)		500 ns
DC offset		<20 mV
PWM frequency		~800 kHz
Error amplifier open loop gain		>60 dB
THD+N* (1kHz, 50W, 4Ω)		0.01 %
Residual Noise* (AES-17 Filter)		200 µVrms

* measured with recommended circuit

Typical Applications

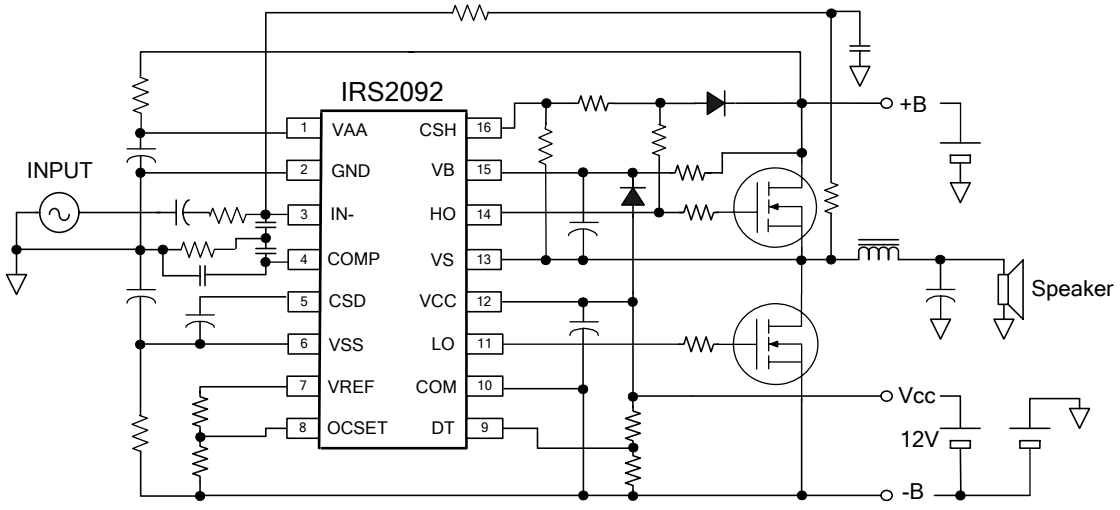
- Home theater systems
- Mini component stereo systems
- Powered speaker systems
- General purpose audio power amplifiers

Package Options

SOIC16N

PDIP16

Typical Connection Diagram



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Description

The IRS2092 is a high voltage, high performance Class D audio amplifier driver with PWM modulator and protection. In conjunction with two external MOSFET and a few external components, a complete Class D audio amplifier with protection can be realized.

International Rectifier's proprietary noise isolation technology allows high current gate drive stage and high speed low noise error amplifier reside on a single small silicon die.

Open elements of PWM modulator section allow flexible PWM topology implementation.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V_B	High side floating supply voltage		-0.3	220	V
V_S	High side floating supply voltage (Note2)		V_B -20	V_B +0.3	
V_{HO}	High side floating output voltage		V_S -0.3	V_B +0.3	
V_{CSH}	CSH pin input voltage		V_S -0.3	V_B +0.3	
V_{CC}	Low side fixed supply voltage (Note2)		-0.3	20	
V_{LO}	Low side output voltage		-0.3	Vcc+0.3	
V_{AA}	Floating input positive supply voltage (Note2)		(See I_{AAZ})	210	
V_{SS}	Floating input negative supply voltage (Note2)		-1 (See I_{SSZ})	GND +0.3	
V_{GND}	Floating input supply ground voltage		V_{SS} -0.3 (See I_{SSZ})	V_{AA} +0.3 (See I_{AAZ})	
I_{IN-}	Inverting input current (Note1)		---	±3	mA
V_{CSD}	SD pin input voltage		V_{SS} -0.3	V_{AA} +0.3	V
V_{COMP}	COMP pin input voltage		V_{SS} -0.3	V_{AA} +0.3	
V_{DT}	DT pin input voltage		-0.3	V_{CC} +0.3	
V_{OCSET}	OCSET pin input voltage		-0.3	V_{CC}+0.3	
I_{AAZ}	Floating input positive supply zener clamp current (Note2)		---	20	mA
I_{SSZ}	Floating input negative supply zener clamp current (Note2)		---	20	
I_{CCZ}	Low side supply zener clamp current (Note3)		---	10	
I_{BSZ}	Floating supply zener clamp current (Note3)		---	10	
I_{OREF}	Reference output current		---	5	
dV_S/dt	Allowable Vs voltage slew rate		---	50	V/ns
dV_{SS}/dt	Allowable Vss voltage slew rate (Note3)		---	50	V/ms
Pd	Maximum power dissipation @ $T_A \leq +25°C$	SOIC16N	---	1.0	W
		DIP16	---	1.6	
Rth_{JA}	Thermal resistance, Junction to ambient	SOIC16N	---	115	°C/W
		DIP16	---	75	
T_J	Junction Temperature		---	150	°C
T_S	Storage Temperature		-55	150	°C
T_L	Lead temperature (soldering, 10 seconds)		---	300	°C

Note1: IN- contains clamping diode to GND.

Note2: V_{DD} – IN+, GND -V_{SS}, V_{CC}-COM and V_B-V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

Note3: For the rising and falling edges of step signal of 10 V. V_{SS}=15 V to 200 V.

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Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at V_{AA}-V_{SS}=10 V, V_{CC}=12 V and V_B-V_S=12 V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S +10	V_S +18	V
V_S	High side floating supply offset voltage	(Note 1)	200	
I_{AAZ}	Floating input positive supply zener clamp current	1	11	mA
I_{SSZ}	Floating input negative supply zener clamp current	1	11	
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High side floating output voltage	Vs	V_B	
V_{CC}	Low side fixed supply voltage	10	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{GND}	GND pin input voltage	V_{SS} (Note 3)	V_{AA} (Note 3)	
V_{IN-}	Inverting input voltage	V_{GND} -0.5	V_{GND} +0.5	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{AA}	
V_{COMP}	COMP pin input voltage	V_{SS}	V_{AA}	
C_{COMP}	COMP pin phase compensation capacitor to GND	1	-	nF
V_{DT}	DT pin input voltage	0	V_{CC}	V
I_{OREF}	Reference output current to COM (Note 2)	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
V_{CSH}	CSH pin input voltage	Vs	V_B	
dVss/dt	Allowable Vss voltage slew rate upon power-up (Note4)	-	50	V/ms
I_{PW}	Input pulse width	10 (Note 5)	-	ns
f_{SW}	Switching Frequency	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for Vs equal to –5 V to +200 V. Logic state held for Vs equal to –5 V to $–V_{BS}$.
Note 2: Nominal voltage for V_{REF} is 5.1 V. I_{OREF} of 0.3 – 0.8 mA dictates total external resistor value on VREF to be 6.3 kΩ to 16.7 kΩ.
Note 3: GND input voltage is limited by I_{AAZ} and I_{SSZ}.
Note 4: V_{SS} ramps up from 0 V to 200 V.
Note 5: Output logic status may not respond correctly if input pulse width is smaller than the minimum pulse width.

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Electrical Characteristics

V_{CC},V_{BS}= 12 V, V_{SS}=V_S=COM=0 V, V_{AA}=10 V, C_L=1 nF and T_A=25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2		
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-		
I_{QCC}	Low side quiescent current	-	-	3	mA	V_{DT}=V_{CC}
V_{CLAMPL}	Low side zener diode clamp voltage	19.6	20.4	21.6	V	I_{CC}=5 mA
High Side Floating Supply						
UV_{BS+}	High side well UVLO positive threshold	8.0	8.5	9.0	V	
UV_{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8		
UV_{BSHYS}	UV_{BS} hysteresis	-	0.2	-		
I_{QBS}	High side quiescent current	-	-	1	mA	
I_{LKH}	High to Low side leakage current	-	-	50	µA	V_B=V_S =200 V
V_{CLAMPH}	High side zener diode clamp voltage	19.6	20.4	21.6	V	I_{BS}=5 mA
Floating Input Supply						
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	V_{SS} =0 V, GND pin floating
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7		V_{SS} =0 V, GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-		V_{SS} =0 V, GND pin floating
I_{QAA0}	Floating Input positive quiescent supply current	-	0.5	2	mA	V_{AA}=10 V, V_{SS} =0 V, V_{CSD} =VSS
I_{QAA1}	Floating Input positive quiescent supply current	-	8	11		V_{AA}=10 V, V_{SS} =0 V, V_{CSD} =VAA
I_{QAA2}	Floating Input positive quiescent supply current	-	8	11		V_{AA}=10 V, V_{SS} =0 V, V_{CSD} =GND
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100 V
$V_{CLAMPM+}$	V_{AA} floating supply zener diode clamp voltage, positive, with respect to GND	6.0	7.0	8.0	V	I_{AA}=5 mA, I_{SS}=5 mA, V_{GND}=0 V, V_{CSD} =VSS
$V_{CLAMPM-}$	V_{SS} floating supply zener diode clamp voltage, negative, with respect to GND	-8.0	-7.0	-6.0		I_{AA}=5 mA, I_{SS}=5 mA, V_{GND}=0 V, V_{CSD} =VSS
Audio Input (V_{GND}=0, V_{AA}=5V, V_{SS}=-5V)						
V_{OS}	Input offset voltage	-15	0	15	mV	
I_{BIN}	Input bias current	-	-	40	nA	
BW	Small signal bandwidth	-	9	-	MHz	C_{COMP}=2 nF, Rf=3.3 kΩ
V_{COMP}	OTA Output voltage	VAA-1	-	VSS+1	V	
g_m	OTA transconductance	-	100	-	mS	V_{IN-}=10 mV
G_V	OTA gain	60	-	-	dB	
V_{Nrms}	OTA input noise voltage	-	250	-	mVrms	BW=20 kHz, Resolution BW=22 Hz Fig.5
SR	Slew rate	-	±5	-	V/us	C_{COMP}=1 nF
CMRR	Common-mode rejection ratio	-	60	-	dB	
PSRR	Supply voltage rejection ratio	-	65	-		
PWM comparator						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA}-V_{SS})/2	-	V	
f_{OTA}	COMP pin star-up local oscillation	0.7	1.0	1.5	MHz	V_{CSD} =GND

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	frequency					

Protection						
V_{REF}	Reference output voltage	4.8	5.1	5.4	V	I_{OREF} =0.5 mA
Vth_{OCL}	Low side OC threshold in Vs	1.1	1.2	1.3		OCSET=1.2 V, Fig.6
Vth_{OCH}	High side OC threshold in V_{CSH}	1.1+ Vs	1.2+ Vs	1.3+ Vs		Vs=200 V,
Vth1	CSD pin shutdown release threshold	$0.62xV_{AA}$	$0.70xV_{AA}$	$0.78xV_{AA}$		
Vth2	CSD pin self reset threshold	$0.26xV_{AA}$	$0.30xV_{AA}$	$0.34xV_{AA}$		
I_{CSD+}	CSD pin discharge current	70	100	130	µA	$V_{CSD} = V_{SS}$ +5 V
I_{CSD-}	CSD pin charge current	70	100	130		$V_{CSD} = V_{SS}$ +5 V
t_{SD}	Shutdown propagation delay from $V_{CSD} > V_{SS} + Vth_{OCH}$ to Shutdown	-	-	250	ns	
t_{OCH}	Propagation delay time from $V_{CSH} > Vth_{OCH}$ to Shutdown	-	-	500		Fig.3
t_{OCL}	Propagation delay time from Vs> Vth_{OCL} to Shutdown	-	-	500		Fig.4
Gate Driver						
Io+	Output high short circuit current (Source)	-	1.0	-	A	Vo=0 V, PW≤10 µs
Io-	Output low short circuit current (Sink)	-	1.2	-	A	Vo=12 V, PW≤10 µs
V_{OL}	Low level out put voltage LO – COM, HO - VS	-	-	0.1	V	Io=0 A
V_{OH}	High level out put voltage VCC – LO, VB - HO	-	-	1.4		
ton	High and low side turn-on propagation delay	-	360	-	ns	$V_{DT} = V_{CC}$
toff	High and low side turn-off propagation delay	-	335	-		$V_{DT} = V_{CC}$
tr	Turn-on rise time	-	20	50		
tf	Turn-off fall time	-	15	35		
DT1	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	15	25	35		$V_{DT}>V_{DT1,}$
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	25	40	55		$V_{DT1}>V_{DT}> V_{DT2,}$
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	50	65	85		$V_{DT2}>V_{DT}> V_{DT3,}$
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})$V_{DT}= V_{DT4}$	85	105	135		$V_{DT3}>V_{DT}> V_{DT4,}$
V_{DT1}	DT mode select threshold 2	0.51xVcc	0.57xVcc	0.63xVcc	V	
V_{DT2}	DT mode select threshold 3	0.32xVcc	0.36xVcc	0.40xVcc		
V_{DT3}	DT mode select threshold 4	0.21xVcc	0.23xVcc	0.25xVcc		

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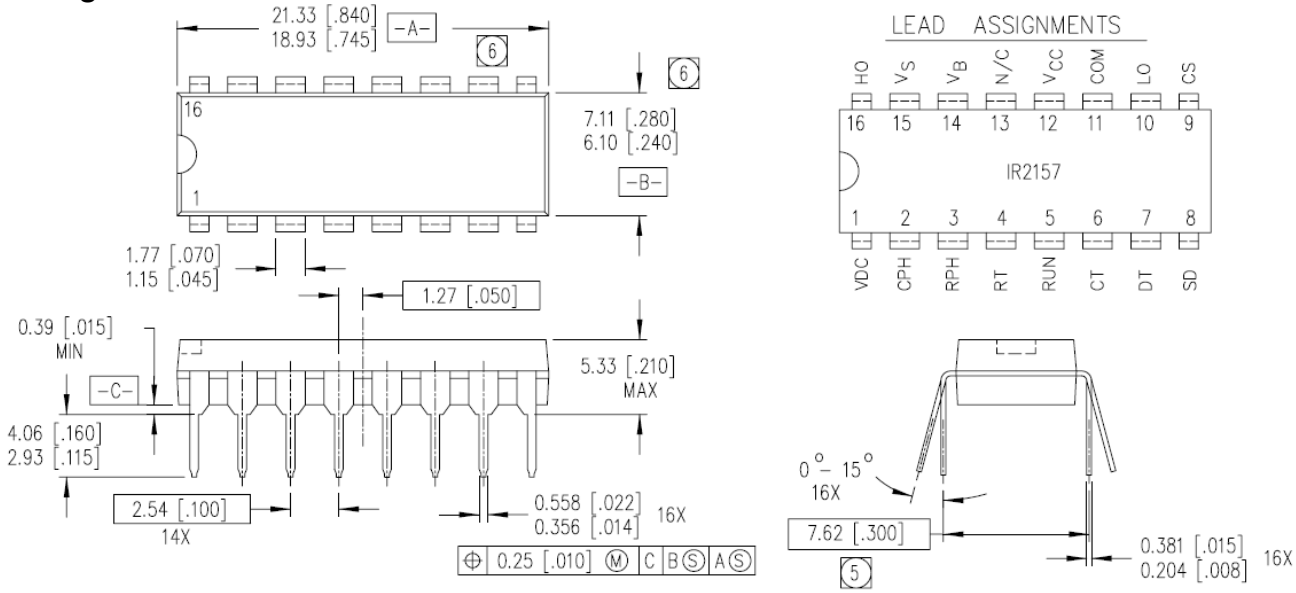
Package Details: PDIP16



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.

2 CONTROLLING DIMENSION: INCH.

3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.

(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

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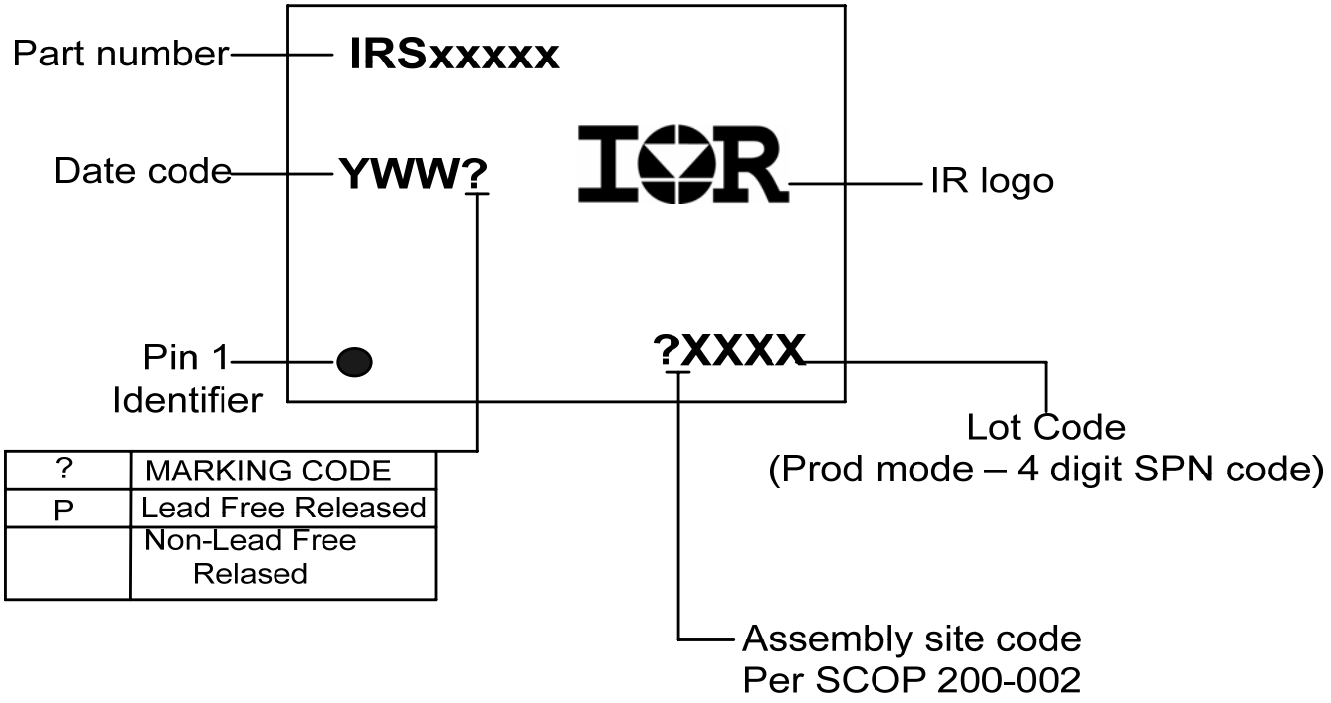
Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

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Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2092	PDIP16	Tube/Bulk	25	IRS2092PBF
	SOIC16N	Tube/Bulk	45	IRS2092SPBF
		Tape and Reel	2500	IRS2092STRPBF

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